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Planar junction formation in HgCdTe infrared detectors

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This paper presents an overview of fundamental techniques for planar junction formation in HgCdTe infrared detectors. At the beginning, the evolution of HgCdTe photodiode performance is presented. Further considerations are restricted to modern methods of p-n junction formation, so the current state of the art of different types of HgCdTe photodiodes is presented. The comparison of theoretical and experimental results for planar HgCdTe photodiodes is finally described.

Keywords: planar photodiodes, heterojunction, HgCdTe.

1. Introduction

At present, HgCdTe is the most widely used variable gap semiconductor for infrared (IR) photodetectors. Over the years it has successfully fought off major challenges from extrinsic silicon and lead-tin telluride devices, but despite that it has more competitors today than ever before. These include Schottky barriers on silicon, SiGe heterojunctions, AlGaAs multiple quantum wells, GaInSb strain layer superlattices, high temperature superconductors and especially two types of thermal detectors: pyroelectric detectors and silicon bolometers. It is interesting, however, that none of these competitors can compete in terms of fundamental properties [1,2]. They may promise to be more manufacturable, but never to provide higher performance or, with the exception of thermal detectors, to operate at higher or even comparable temperatures.

The specific advantages of HgCdTe are the direct energy gap, ability to obtain both low and high carrier concentrations, high mobility of electrons and low dielectric constant. The extremely small change of lattice constant with composition makes it possible to grow high quality layers and graded gap structures. HgCdTe can be used for detectors operated at various modes, and can be optimised for operation at the extremely wide range of the IR spectrum (1–30 μm) and at the temperatures ranging from that of liquid helium to the room temperature.

Initially, the photodiodes were prepared from bulk materials which performance were next considerably improved. Further development was, however, dominated by various epitaxial techniques including ISOVPE, LPE, MBE, and MOCVD. In more technologies, the junction at the semiconductor surface is exposed during device processing. The exposure of the junction surface can affect uniformity and yield. The planar structures with the junction buried beneath the top wide gap layer overcome the technologically difficult passivation stage [3].

Here, we will review the recent trends in $Hg_{1-x}Cd_xTe$ photodiodes with the major emphasis on the means to improve performance of the planar devices. More attention is paid on p–n heterojunction photodiodes because of their importance in focal plane arrays (FPAs). Finally, the main characteristics of the planar photodiodes are presented.

2. Evolution of HgCdTe photodiode architecture

A variety of HgCdTe photodiode configurations have been proposed including mesa, planar and lateral n-p, n^+-n-p, p-n, n^+-p homojunction and heterojunction structures (the n-p stands for a thick p-type matrix with a thin n-type surface layer) [4]. The p-n junctions have been formed by numerous techniques including Hg in- and out-diffusion, impurity diffusion, ion implantation, electron bombardment, doping during growth from vapour of liquid phase and other methods.

The fabrication of HgCdTe photodiodes was usually based on the most common n^+-p [5] and P^+-n structure [6]. In these diodes, the lightly doped narrow gap absorbing region ("base" of the photodiode), determines the dark current and photocurrent. The base p-type layers (or n-type layers) are sandwiched between CdZnTe substrate and high-doped (in n^+-p structures) or wider-gap (in P^+-n structure) regions. Due to the backside illumination (through CdZnTe or Si substrate) and internal electric fields (which are "blocking" for minority carriers), influence of surface recombinations on the photodiodes performance is eliminated. Neither n^+-region nor P^+-region contributes to the dark current. Both optical and thermal generations are suppressed in the n^+-region due to the Burstein-Moss effect and in the P^+-region due to a wide gap. Since the base region determines largely the properties of the device, it should be carefully optimised. The thickness of the base re-

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gion should be optimised for near unity quantum efficiency and a low dark current. This is achieved with a base thickness slightly higher than the inverse absorption coefficient for single pass devices: $t = 1/\alpha$ (which is $\approx$10 μm) or half of the $1/\alpha$ for double pass devices (devices supplied with a retroreflector). Low doping is beneficial for a low thermal generation and high quantum efficiency. Since the diffusion length in absorbing region is typically longer than its thickness, any carriers generated in the base region can be collected giving rise to the photocurrent. Recently, this effect has been used in lateral collection device with a small central contact called loophole device [7].

The heterojunction mesa technology is rather straightforward, but it can be difficult to control the passivation process, especially for small-area devices typically used for imaging applications. An important development in the evolution of HgCdTe photodiode technology is the capability to grow double layer heterostructures with formation of planar photodiodes by implantation [3]. Figure 1 shows the schematic diagram of evolution of HgCdTe photodiode architecture as a function of time.

3. Technology

The low binding energies and ionic bond nature of HgCdTe give rise to two important effects that are influential in most junctions forming processes. The first is the role of Hg which is liberated readily by the processes such as ion implantation and ion beam milling. This creates a much deeper junction than would be expected from the implantation range. A second effect is the role of dislocations that may play a part in annihilating vacancies. The role of Hg interstitials, dislocations and ion bombardment in the junction forming process is complex and not well understood in detail. Despite the complex physics involved, manufactures have received good phenomenological control of the junction depth and n-dopant profiles with a variety of processes.

3.1. Ion implantation

The ion implantation in HgCdTe is well-established approach for fabricating HgCdTe photovoltaic devices with n-on-p type junctions [8]. It is a common method of HgCdTe photodiode fabrication since it avoids heating of this metallurgically sensitive material and permits a precise control of a junction depth. Many manufacturers obtain the desired p-type level by controlling the density of acceptor-like Hg vacancies within a carrier concentration range of 10^{16} to 10^{17} cm^{-3}. The n^+-p structures are produced by Al, Be, In and B ions implantation into vacancy doped p–type material, but the technique typically uses ion implantation of light species (usually B and Be) to form n-region. Boron is possibly the most frequently used, perhaps due to the fact that boron is also a standard implant for silicon.

For planar devices, prior to implantation, the substrates are covered with the dielectric layers (photoresists, ZnS, CdTe) with openings acting as a mask for impinging ions and thus defining the junction area. Implantation is typically performed at the room temperature; the substrates, if oriented, are inclined to the beam axis to avoid ion channelling. The doses of 10^{12}–10^{15} cm^{-2} and energies of 30–200 keV are applied. No post-implant annealing was found to be necessary to achieve high performance, particularly at the lower doses and for SWIR and MWIR devices. Some workers concluded that LWIR photodiode performance can be improved if postimplant annealing is used [9]. The post-implant anneals remove the radiation damage with a temperature dependence which varies with implanted species and with implant/anneal conditions.

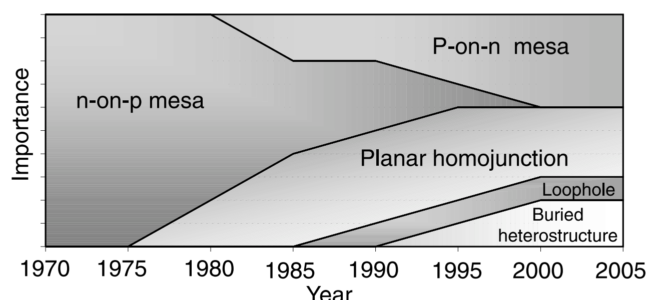

Fig. 1. Schematic diagram of evolution of HgCdTe photodiode architecture as a function of time.

The planar device structure illustrated in Fig. 2 is the simplest device structure currently used. To overcome the problem with hybridisation, producible alternative to CdTe for epitaxy (PACE) technology is being developed with sapphire or silicon as the substrate of HgCdTe detectors. A layer of CdTe is grown via MOCVD on the sapphire. HgCdTe is then grown on the CdTe buffer via LPE. The detector array is backside illuminated through the sapphire substrate which transmits to 6.5 m for a 7-mil thickness. The junctions are formed by boron ion implantation and thermal annealing. The planar junctions are passivated with a ZnS or CdTe film. The PACE process currently provides intrinsic detector arrays with BLIP performance and a satisfactory yield. The metal contacts and indium columns are then deposited and patterned on both detector array and the multiplexing readout, and the hybrid is fabricated by mat-

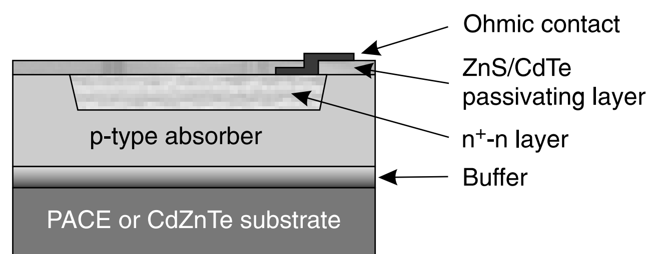

Fig. 2. Cross sectional view of the planar HgCdTe ion implanted photodiode.

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ing the detector array to the readout via indium column interconnects. The sapphire substrate offers several attributes. Its thermal coefficient of expansion matches well to the alumina chip carrier, thereby greatly improving large hybrid reliability. The large substrate also reduces detector cost by increasing throughput, enabling batch processing and reducing breakage. The 3 inch wafers currently in production allow for populating each wafer with either five 18.5-μm pixel 1024×1024 arrays (in addition to four 40-μm 256×256 arrays), eight 27-μm 640×480 arrays, or twenty one 256×256 arrays.

A plasma induced type conversion in HgCdTe, as an alternative to ion implantation junction formation technology, has received considerable attention during the past few years [10]. The post-implant annealing, necessary in implantation technology to produce high-quality photodiodes, is not needed in the plasma technology. Reactive ion etching (RIE) induced type conversion and junction formation have been observed in a vacancy doped p-MCT using H_2/CH_4. The etch depth has been investigated as a function of the partial pressure of H_2 and CH_4 and it reaches a maximum at about 0.8 hydrogen level. The junction depth could be adjusted from 2–20 μm. Long wave infrared diodes have been fabricated with the average R_0A of 50 Ω cm^2. The devices were found to be stable at a baking temperature of 80°C over a period of ten days.

3.2. Loophole planar technique

Via-hole devices have been commercially produced since 1980 and they are known as loophole devices or via interconnected photodiode (VIP) devices. The loophole device is illustrated in Fig. 3. This is a lateral collection device with a small central contact. The photosensitivity is by absorption in the n and p-regions and diffusion to the junction. By using a thin monolith of HgCdTe bonded rigidly to the silicon, the thermal expansion mismatch problem is overcome because the strain is taken up elastically. The process has two simple masking stages. The first defines a photoresist film with a matrix of the holes. Using ion beam milling, the HgCdTe is eroded away in the holes until the contact pads are exposed. The holes are then backfilled with a conductor to form the bridge between the walls of the hole and the underlying metal pad. The junction is formed around the hole during the ion beam milling process. The second masking stage enables the p-side contact to be applied around the array.

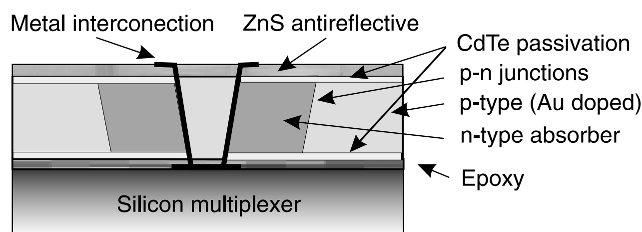

Fig. 3. n-p loophole HgCdTe homojunction photodiode architecture.

The high density VIP (HDVIP) process results in similar structure but uses a plasma etching stage to cut the via-hole and an ion implantation stage to create a stable junction and a damage region near the contact [11]. In via-hole processes, cylindrical shape of the junction minimises the intersection with the threading dislocations. The detector itself is a front side illuminated, n/p diode fabricated on a thinned, extrinsic-doped, p-type HgCdTe epilayer. The controlled intrinsic and extrinsic doping is used to optimise the material lifetime, diffusion length, and dark current level at the given N_A in the epitaxial film.

3.3. Planar heterostructure

Mesa heterostructures are effective for reducing the thermal leakage currents in small photodiodes. They have, however, a technologically difficult passivation stage on the sidewalls of the mesa, which can lead to reverse bias leakage and uniformity problems if not optimum. Arias *et al.* [3] have demonstrated a clever diffused heterostructure, which overcomes the sidewall problem called double-layer planar heterostructure (DLPH). The benefits of the DLPH architecture include a reduction in tunnelling current and surface generation-recombination currents. Those benefits are realized by incorporating a buried narrow-bandgap active layer in the DLPH architecture. The planar devices were formed using a $Hg_{1-y}Cd_yTe$/ /$Hg_{1-x}Cd_xTe$ ($y > x$) heterostructure grown by molecular beam epitaxy. In Fig. 4(a), a scheme of the planar HgCdTe diode heterostructure is shown. An important aspect of the DLPH approach is a planar p-doped/n-doped device geometry that includes a wide-bandgap cap layer over a narrow-bandgap base layer (which is the active layer). The formation of planar photodiodes was achieved by first, selective implanting of arsenic through a ZnS mask and then, diffusing the arsenic (by annealing at high temperature) through the cap layer into the narrow gap base layer. The selective implantation of arsenic was carried out at the room temperature. After the structure was selectively implanted, it was annealed under Hg overpressure in a high-pressure system. The first annealing was carried out to diffuse the arsenic into the base layer and to make the doped region p-type by substitution of arsenic atoms on the Te sublattice, while the second one was carried out to annihilate Hg vacancies formed in the HgCdTe lattice during growth and diffusion of arsenic. Using this technique, the planar devices were fabricated of the following areas: 30×30–500×500 μm^2. The planar devices were further protected [as illustrated in Fig. 4(a)] with a polycrystalline CdTe (thickness 1 μm) deposited at the room temperature in an e-beam system. The electrical contacts were made with alloyed gold on the top of the p-type capping layer and with indium on the n-type layer. To reduce the series resistance, the back wide gap N-type layer is frequently applied.

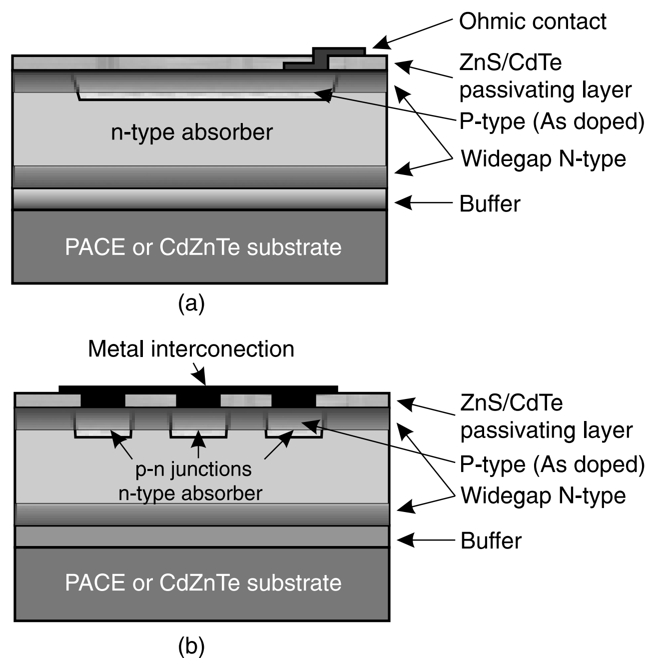

Fig. 4. Schematic drawing of the planar DLPH HgCdTe diode heterostructure: conventional configuration (a) and lateral current-collection configuration (b).

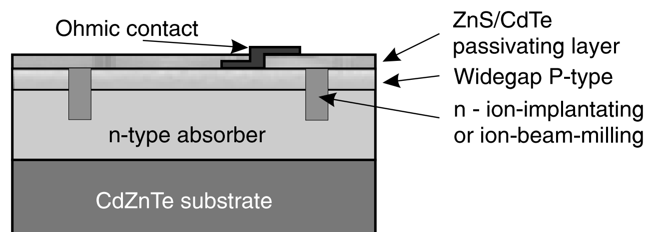

Fig. 5. Schematic cross section of the PI_3H HgCdTe photodiode.

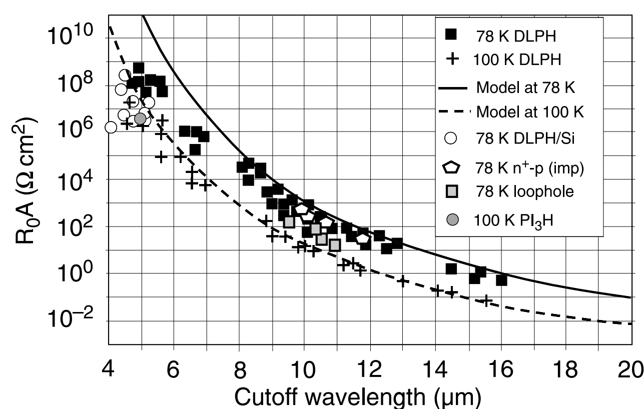

Fig. 6. Dependence of the R_0A product on the long wavelength cut-off for planar HgCdTe photodiodes at 77 and 100 K. The experimental values are taken from Refs. 5, 11, 12,13, and 14.

With a proper design the DLPH, the optical collection area of a detector can be substantially larger than its electrical junction area [Fig. 4(b)]. Instead of one diode, each detector pixel contains several diodes formed as small-area implants separated by a distance of the order of one minority-carrier diffusion length and electrically connected in parallel via their ohmic contacts. Following this approach to design and fabrication, optical detection areas can be an order of magnitude greater than the electrical junction areas and advantages of reduced dark current, relatively high resistance, and relatively low capacitance can be realised. Decreasing junction area indirectly increases device yield by reducing the probability that a given defect will coincide with a junction.

3.4. Planar configuration in doping during growth structures

High-performance photodiodes can be obtained by a successive growth of the doped layers using LPE, MBE, and MOCVD. Doping during growth makes it possible to grow multilayer structures. Recently, these techniques are most often used for preparing the mesa and planar p-on-n junctions.

As it was mentioned in Ref. 3, the As dopants must reside on the Te site to accomplish p-doping. This requires either growth or annealing at the relatively high temperatures under cation-rich conditions. LPE growth from an Hg melt (at the temperature around 400°C) satisfies this condition automatically, although some post growth annealing may be required. MOCVD and MBE have been successfully accomplished As doping during the growth.

To take advantage of the strengths of the boron implantation and the heterojunction epitaxy techniques, the planar ion implantation isolated heterojunction (PI_3H) process has been developed for producing the HgCdTe photodiodes [12]. Figure 5 depicts the PI_3H diode structure. The heterostructure double layers are first grown. Then, CdTe passivation layer is deposited onto the surface of the layer, followed by a thermal treatment. Finally, ion implantation is applied using photolithography to isolate the heterojunction layer into discrete diodes. Bahir *et. al.* [13] have developed a new process that omits the ion-implantation step and permits formating a controllable and relatively deep junction which is used to isolate the planar p-on-n heterojunction photodiodes. The planar technology was based on ion-beam milling to induce conductivity-type conversion in order to form a lateral n-p junction in the p-type cap material. A detail analysis of the current characteristics of these diodes as a function of temperature show that their dark current is diffusion-limited down to 60 K. The new planar technology significantly simplifies the process of photodiodes fabrication as well as fabrication of a state-of-art 2-D array is possible.

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4. Properties of HgCdTe planar photodiodes

The electrical performance of a photodiode is characterised by its electrical current-voltage behaviour and the optical performance is characterised by its quantum efficiency and spectral response. For the detectors, the normalized figure of merit indicative of noise (and, consequently, sensitivity) is R_oA, the zero-bias detector impedance, area product. HgCdTe planar photodiodes operated at 77 K with R_oA product much higher than that required for BLIP performance have been obtained by a number of methods. Figure 6 shows the dependence of the R_oA product on the long wavelength cutoff for HgCdTe photodiodes at 78 K and 100 K. The dashed and solid lines are the theoretical R_oA product, calculated using a one-dimensional model that assumes diffusion-current domination from the base layer, and minority carrier recombination-generation is via Auger and radiative processes [14]. Typical values for n-side donor concentration $N_d = 1\times10^{15}$ cm^{-3} was used in theoretical calculations. This figure also includes the experimental data reported by many authors for planar structures. Comparing the measured and theoretically predicted R_oA values we can see that the best DLPH photodiodes exhibit a performance which is very close to the limits set by the Auger generation. The ion implanted n^+-p homojunction achieves the comparable results. The data shows that the experimental R_oA values are equal to, or within a factor of 2, below the theoretical curve for the LWIR detectors. The photodiodes with a lower performance usually contain metallurgical defects such as dislocation clusters and loops, pinholes, striations, Te inclusions, and heavy terracing. The diodes with the highest performance at 78 K contain no visible defects (Hg interstitials and vacancies). Conversely, for MWIR photodiodes, the R_oA product is generally inferior, especially for the structures grown on Si substrates. These problems are probably caused by tunnel and surface currents generated by high density of dislocations at the HgCdTe-grown on Si. The R_oA values for the Au-doped HDVIP detectors are only a factor of 2.7 below the theoretical model. The R_oA values of the diodes formed by PI_3H technique will follow the theoretical curve without bending at low temperatures but no measurements have been conducted, yet.

The high-quality photodiodes operated at 78 K exhibit quantum efficiencies close to the reflection limit or to 100% with antireflection coatings. Because the smaller photodiodes (with radii in the 20–50 μm range) have dimensions comparable to the carrier diffusion length in the base layer, lateral optical collection of photogenerated carriers must be taken into account.

5. Conclusions

Device processing of the planar structures has fewer requirements for surface passivation because the junction interface is buried. An ion implantation is very well adapted to introducing a controlled amount of damage (in n-on-p homojunctions) or As dopand (in P^+-n heterojunctions) and it is compatible with the standard masking techniques used in semiconductor microelectronics. A considerable progress in photovoltaic detectors of this type has been demonstrated by the research groups at Rockwell Science Centre [15] and SOFRADIR [16]. While ion implantation requires activation of the implanted atoms, at relatively high temperatures, an alternative technology (ion milling or plasma induce type conversion) has received considerable attention during the past few years. LWIR devices with performances close to the theoretical limit have been demonstrated for cut-off wavelengths from 9 to 12 μm.

During the past several years, the progress has been made in the growth of MBE and MOCVD CdTe on silicon substrates as well as MBE- and MOCVD-HgCdTe growth on these alternative substrates. In future, it is envisaged that HgCdTe planar photodiodes will be grown directly on silicon or even silicon multiplexers for the very low cost detectors. Band-gap engineering will produce heterostructure detectors with much higher operating temperatures. The device structures will be extended to produce bi-spectral and multi-spectral capability.

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